L Number	Hits	Search Text	DB	Time stamp
-	3	(6420271|6492271|5313633).pn.	USPAT	2004/07/01 10:52
-	1	5923865.pn.	USPAT	2004/07/01 12:34
-	1	6130551.pn.	USPAT	2004/07/01 12:34
-	446	703/22.ccls.	USPAT; US-PGPUB; EPO; JPO	2004/07/01 13:18
-	23	703/22.ccls. and (FPGA or field adj programmable adj gate adj array or programmable adj gate adj array)	USPAT; US-PGPUB; EPO; JPO	2004/07/01 13:19
-	14	(703/22.ccls. and (FPGA or field adj programmable adj gate adj array or programmable adj gate adj array)) and emulat$3	USPAT; US-PGPUB; EPO; JPO	2004/07/01 13:23
-	377	703/23.ccls.	USPAT; US-PGPUB; EPO; JPO	2004/07/01 13:23
-	59	703/23.ccls. and (programmable adj gate adj array or FPGA)	USPAT; US-PGPUB; EPO; JPO	2004/07/01 13:23
-	30	(703/23.ccls. and (programmable adj gate adj array or FPGA)) and (synthesiz$4 or map$4)	USPAT; US-PGPUB; EPO; JPO	2004/07/01 14:05
-	2673	326/38-41.ccls.	USPAT; US-PGPUB; EPO; JPO	2004/07/01 14:08
-	1022	326/38-41.ccls. and (programmable adj gate adj array or FPGA)	USPAT; US-PGPUB; EPO; JPO	2004/07/01 14:09
-	275	(326/38-41.ccls. and (programmable adj gate adj array or FPGA)) and (emulat$3 or simulat$3 or verification)	USPAT; US-PGPUB; EPO; JPO	2004/07/01 14:10
-	158	((326/38-41.ccls. and (programmable adj gate adj array or FPGA)) and (emulat$3 or simulat$3 or verification)) and (synthes$4 or map$3 or compil$2)	USPAT; US-PGPUB; EPO; JPO	2004/07/01 14:11
-	87	(((326/38-41.ccls. and (programmable adj gate adj array or FPGA)) and (emulat$3 or simulat$3 or verification)) and (synthes$4 or map$3 or compil$2)) and (LUT or look adj up adj table)	USPAT; US-PGPUB; EPO; JPO	2004/07/01 14:12
-	75	((((326/38-41.ccls. and (programmable adj gate adj array or FPGA)) and (emulat$3 or simulat$3 or verification)) and (synthes$4 or map$3 or compil$2)) and (LUT or look adj up adj table)) and logic	USPAT	2004/07/01 14:12
-	75	(((((326/38-41.ccls. and (programmable adj gate adj array or FPGA)) and (emulat$3 or simulat$3 or verification)) and (synthes$4 or map$3 or compil$2)) and (LUT or look adj up adj table)) and logic) and (interconnect or rout$3 or signal)	USPAT	2004/07/01 14:17
-	2	((((((326/38-41.ccls. and (programmable adj gate adj array or FPGA)) and (emulat$3 or simulat$3 or verification)) and (synthes$4 or map$3 or compil$2)) and (LUT or look adj up adj table)) and logic) and (interconnect or rout$3 or signal)) and log	USPAT	2004/07/01 14:17
-	980	716/4.ccls.	USPAT	2004/07/01 14:40
-	80	716/4.ccls. and (FPGA or field adj programmable adj gate adj array)	USPAT	2004/07/01 14:41
-	59	(716/4.ccls. and (FPGA or field adj programmable adj gate adj array)) and (emulat$3 or simulat$3)	USPAT	2004/07/01 14:41
-	46	((716/4.ccls. and (FPGA or field adj programmable adj gate adj array)) and (emulat$3 or simulat$3)) and (synthesi$3 or map$3)	USPAT	2004/07/01 14:42

-	46	(((716/4.ccls. and (FPGA or field adj programmable adj gate adj array)) and (emulat$3 or simulat$3)) and (synthesi$3 or map$3)) and logic	USPAT	2004/07/01 14:50
-	251	716/13.ccls.	USPAT	2004/07/01 14:50
-	13	716/13.ccls. and (FPGA or field adj programmable adj gate adj array)	USPAT	2004/07/01 14:51
-	5	(716/13.ccls. and (FPGA or field adj programmable adj gate adj array)) and (emulat$3 or simulat$3)	USPAT	2004/07/01 14:54
-	381	716/17.ccls.	USPAT	2004/07/01 14:54
-	141	716/17.ccls. and (FPGA or programmable adj gate adj array)	USPAT	2004/07/01 14:54
-	68	(716/17.ccls. and (FPGA or programmable adj gate adj array)) and (emulat$3 or simulat$3)	USPAT	2004/07/01 14:55
-	51	((716/17.ccls. and (FPGA or programmable adj gate adj array)) and (emulat$3 or simulat$3)) and (synthesi$3 or map$3)	USPAT	2004/07/01 14:55
-	11	(((716/17.ccls. and (FPGA or programmable adj gate adj array)) and (emulat$3 or simulat$3)) and (synthesi$3 or map$3)) and LUT	USPAT	2004/07/01 15:00
-	562	716/18.ccls.	USPAT	2004/07/01 15:00
-	118	716/18.ccls. and (fpga or programmable adj logic adj device)	USPAT	2004/07/01 15:01
-	74	(716/18.ccls. and (fpga or programmable adj logic adj device)) and (emulat$3 or simulat$3)	USPAT	2004/07/01 15:01
-	9	(((716/18.ccls. and (fpga or programmable adj logic adj device)) and (emulat$3 or simulat$3)) and (synthesi$3 or map$3)) and (LUT or look adj up adj table)	USPAT	2004/07/01 15:02
-	67	((716/18.ccls. and (fpga or programmable adj logic adj device)) and (emulat$3 or simulat$3)) and (synthesi$3 or map$3)	USPAT	2004/07/01 15:02
-	19	synthesis and logic and emulation and programmable adj gate adj array and signal and physical and (storage adj unit or lut or look adj up adj table)	USPAT	2004/07/01 15:24
-	408	716/16.ccls.	USPAT; US-PGPUB; EPO; JPO	2004/07/02 15:24
-	275	716/16.ccls. and (PLD or FPGA)	USPAT; US-PGPUB; EPO; JPO	2004/07/02 14:25
-	69	(716/16.ccls. and (PLD or FPGA)) and partitioning	USPAT; US-PGPUB; EPO; JPO	2004/07/02 14:25
-	61	((716/16.ccls. and (PLD or FPGA)) and partitioning) and multiple	USPAT; US-PGPUB; EPO; JPO	2004/07/02 14:25
-	683	716/18.ccls.	USPAT; US-PGPUB; EPO; JPO	2004/07/02 15:25
-	145	716/18.ccls. and (PLD or FPGA)	USPAT; US-PGPUB; EPO; JPO	2004/07/02 15:25
-	75	(716/18.ccls. and (PLD or FPGA)) and partition$3	USPAT; US-PGPUB; EPO; JPO	2004/07/02 15:25
-	68	((716/18.ccls. and (PLD or FPGA)) and partition$3) and multiple	USPAT; US-PGPUB; EPO; JPO	2004/07/02 15:44
-	1027	716/5.ccls.	USPAT; US-PGPUB; EPO; JPO	2004/07/02 15:45
-	71	716/5.ccls. and (PLD or FPGA)	USPAT; US-PGPUB; EPO; JPO	2004/07/02 15:45

-	25	(716/5.ccls. and (PLD or FPGA)) and partition$3	USPAT; US-PGPUB; EPO; JPO	2004/07/02 15:51
-	404	716/7.ccls.	USPAT; US-PGPUB; EPO; JPO	2004/07/02 15:51
-	63	716/7.ccls. and (PLD or FPGA)	USPAT; US-PGPUB; EPO; JPO	2004/07/02 15:51
-	53	(716/7.ccls. and (PLD or FPGA)) and partition$3	USPAT; US-PGPUB; EPO; JPO	2004/07/02 15:51
-	50	((716/7.ccls. and (PLD or FPGA)) and partition$3) and multiple	USPAT; US-PGPUB; EPO; JPO	2004/07/02 15:52
-	206	multi-value adj logic or multi adj value adj logic or multiple adj value adj logic or multiple-valued adj logic	USPAT	2004/07/06 10:01
-	8	(multi-value adj logic or multi adj value adj logic or multiple adj value adj logic or multiple-valued adj logic) and FPGA	USPAT	2004/07/06 10:02

APP # 09779859

7/1/04
Inventor Name Search: EAST, IEEE, ACM, GOOGLE

7/2/04
Talked to Bill Thomson, PRI AU2123
Talked to Kevin Teska, SPE 2123
ACM
+partition +synthesize +logic +LUT +table FPGA PLD

7/6/04
IEEE:
fpga<and>multi value <or>multiple valued
fpga<and>multiple value<and>synthesis
Proceedings 1999 29th IEEE International Symposium on Multiple-Valued Logic (Cat. No.99CB36329)
Proceedings. 1998 28th IEEE International Symposium on Multiple Valued Logic (Cat. No.98CB36138)
Proceedings 1997 27th International Symposium on Multiple- Valued Logi c
Proceedings of 26th IEEE International Symposium on Multiple-Valued Lo gic (ISMVL'96)
Year: 23-25 May 1995
Proceedings 25th International Symposium on Multiple-Valued Logic
Multiple-Valued Logic, 1994. Proceedings., Twenty-Fourth International Symposium on

ACM
+fpga, +lut, +emulate "multiple-valued logic","multi-value logic"
+"multiple-valued logic" fpga emulate

7/7/04
google: hamlet, programmable, "multiple-valued"
ACM: +author:butler +author:j